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(54) Phase/frequency detectors

(57) A phase/frequency detector has first and second inputs (i/p1, i/p2), one of which is converted into a third signal (i) in phase with the first input (i/p1) and a fourth signal (q) in phase quadrature with the second input (i/p2). Gates (A, B) receive the third and fourth signals and the second and fourth signals respectively and feed a current source (I1) and a current sink (I2). A capacitor (C) is connected across the current sink (I2) such that the net charge flowing into the capacitor is defined by the difference between the source and the sink over a given time period. A.C. leakage and "dead band" problems are overcome by the invention.

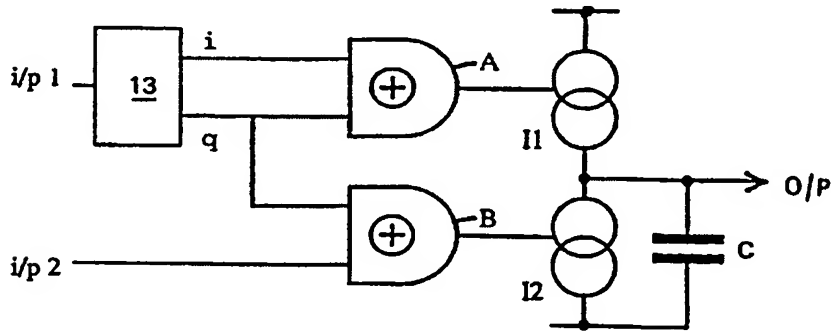

FIG. 4

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

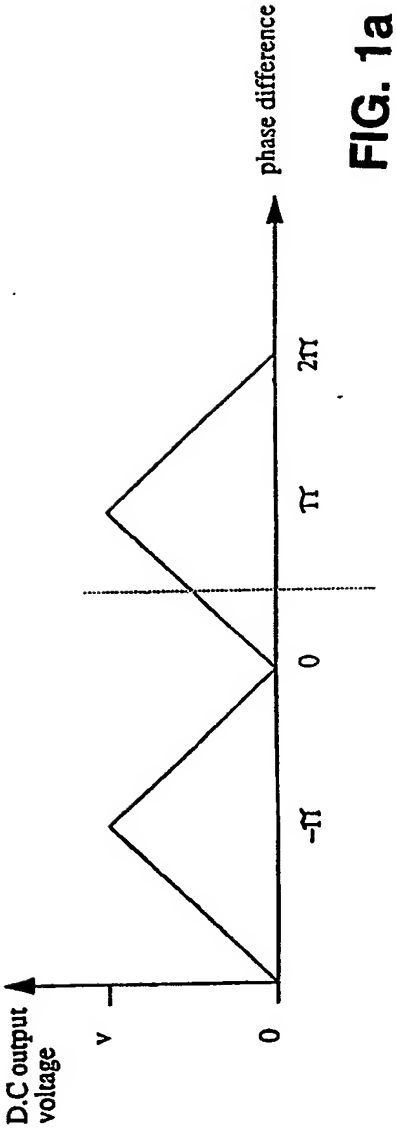
D.C output voltage
V
0
phase difference
-π
0
π
2π

FIG. 1a

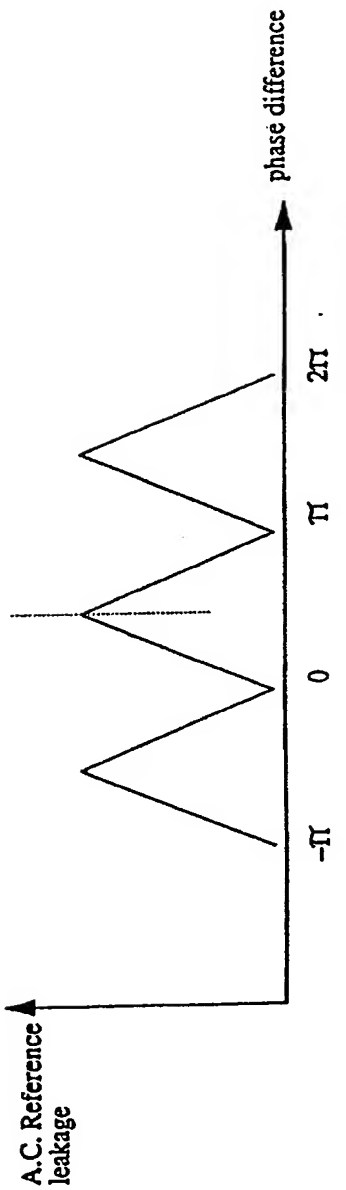
A.C. Reference leakage
phase difference
-π
0
π
2π

FIG. 1b

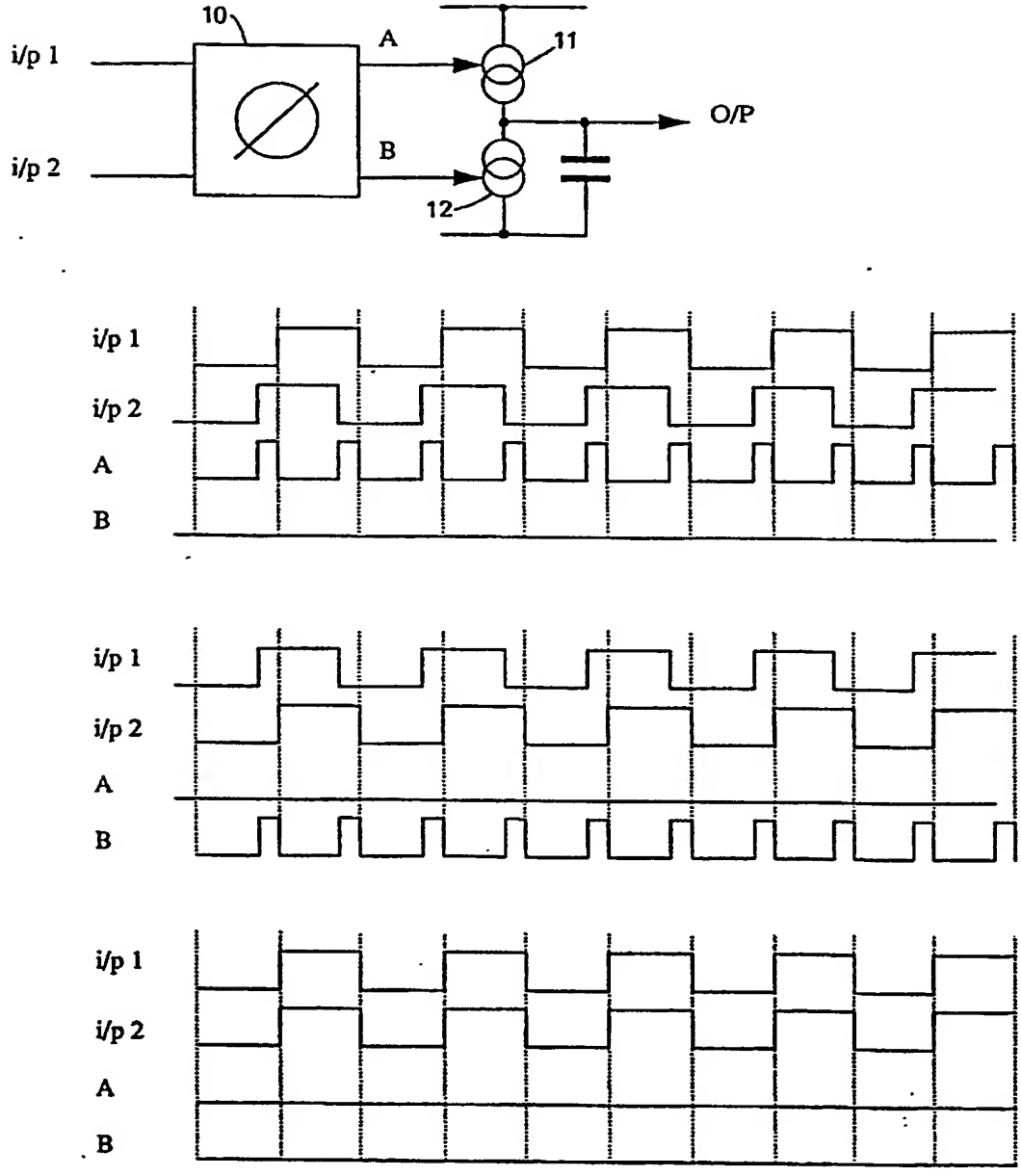

FIG. 2a

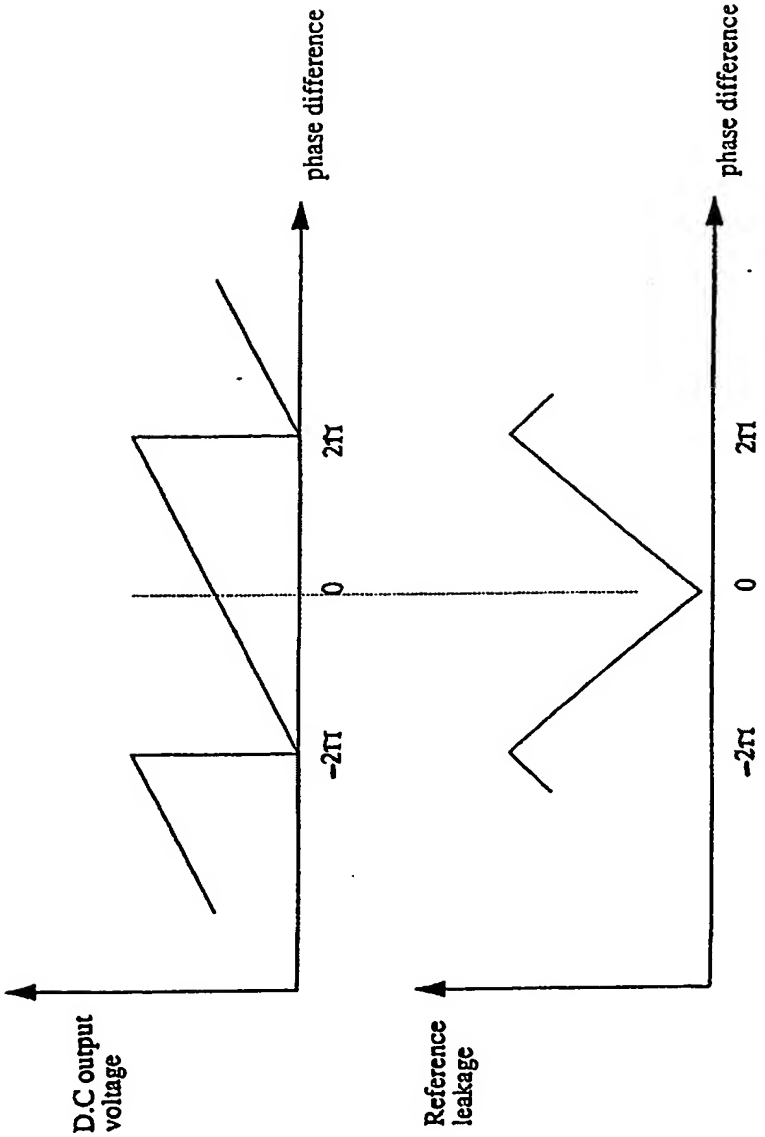
phase difference
2π
0
-2π
D.C output voltage
phase difference
2π
0
-2π
Reference leakage

FIG. 2b

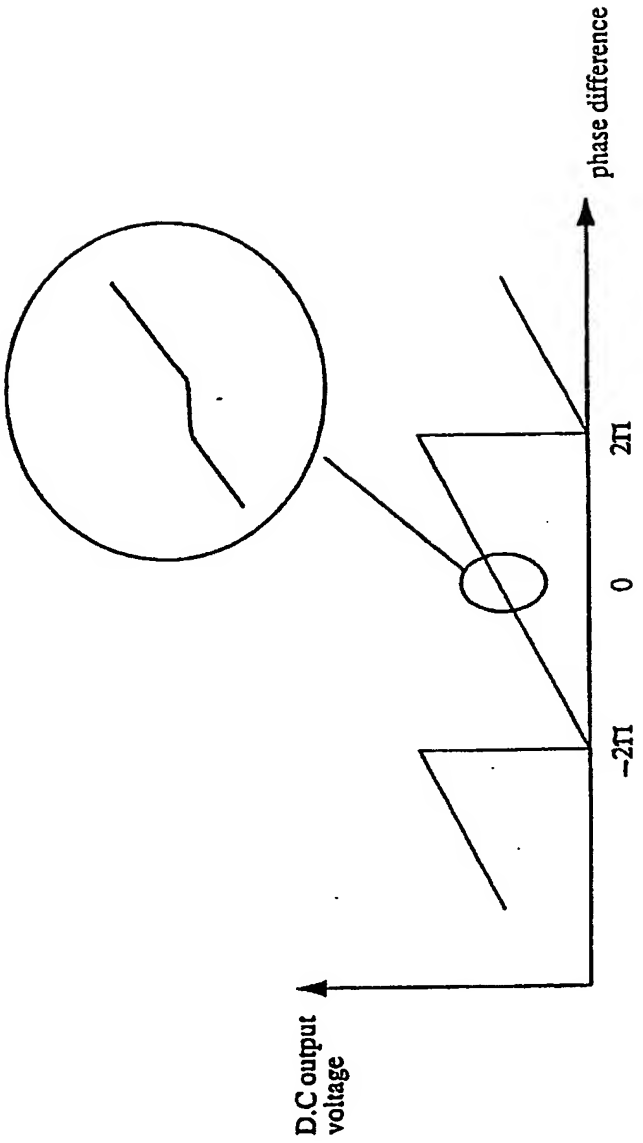

FIG. 3

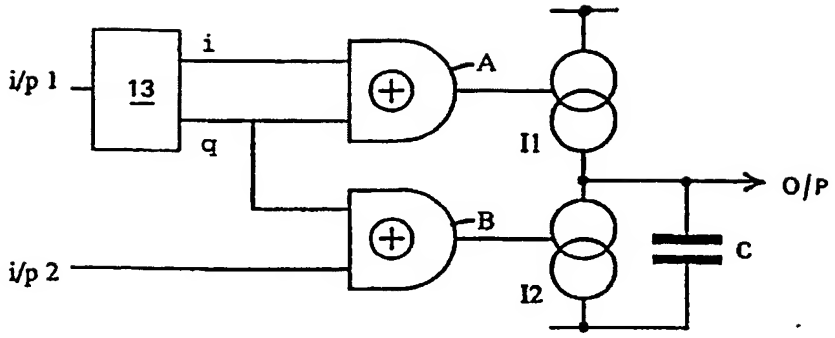
i/p 1
13
i
q
A
B
I1
I2
O/P
C
i/p 2

FIG. 4

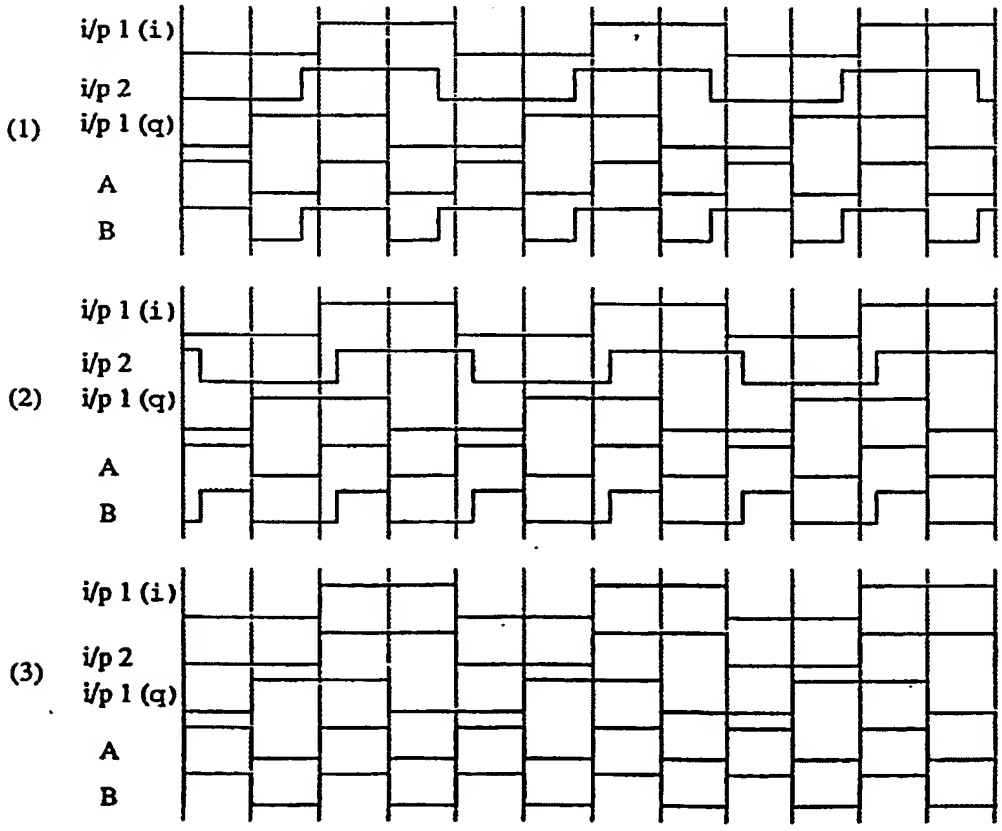
(1)
i/p 1 (i)
i/p 2
i/p 1 (q)
A
B
(2)
i/p 1 (i)
i/p 2
i/p 1 (q)
A
B
(3)
i/p 1 (i)
i/p 2
i/p 1 (q)
A
B

FIG. 5

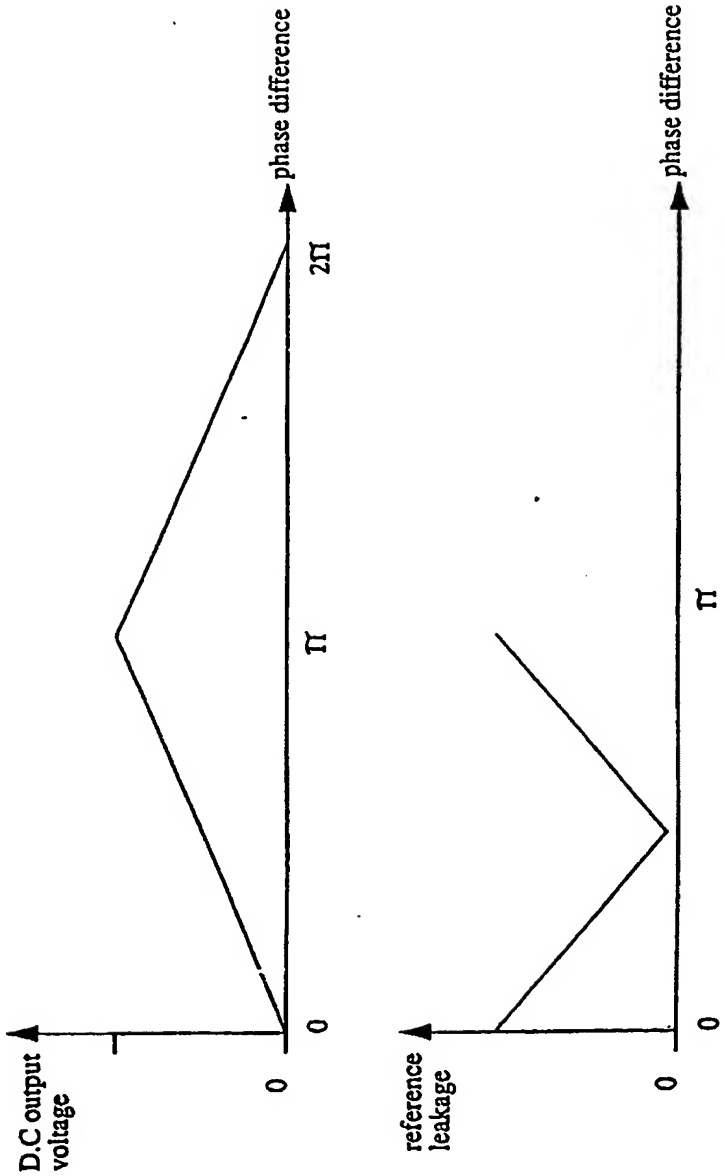
D.C output voltage
0
0
π
2π
phase difference
reference leakage
0
0
π
phase difference

FIG. 6

PHASE/FREQUENCY TO VOLTAGE DETECTORS

This invention relates to phase/frequency to voltage detectors, and to phase locked loop synthesisers which incorporate such detectors.

It is an object of the present invention to provide a detector of this type, and a synthesiser incorporating such a detector, which has significantly improved performance as compared with existing detectors.

One commonly used device for converting phase/frequency to voltage is an exclusive OR device. The phase/voltage characteristic of such a device is shown in Fig. 1a of the accompanying drawings. The phase difference between two input signals is plotted as the abscissa and the d.c. output voltage as the ordinate. The main disadvantage of such a detector is the amount of AC signal leakage. This leakage is at a maximum in the centre of the linear range, as is illustrated by Fig. 1b, where the a.c. leakage is plotted against the phase difference. The centre of the linear range is when the two input signals are in phase quadrature. If the two input signals are of identical frequency, but have a phase difference ϕ in the range $0 < \phi < \pi$, then the fundamental frequency of any AC leakage at the output will be twice that of the input.

An alternative known phase/frequency to voltage detector is a digital tri-state detector, the operation of which is illustrated by Figs. 2a and 2b of the accompanying drawings. In Fig. 2a the two inputs i/p1 and i/p2 are two signals with an arbitrary phase difference between them, but of the same frequency. These signals are fed to a logic circuit 10 of gates which has outputs A and B, one to a current source 11 and the other to a current sink 12 of a charge pump. A

and the other to a current sink 12 of a charge pump. A capacitor C is connected across the current sink 12. This detector gives good suppression of any AC components at the output O/P when in the centre of its linear range, i.e. no phase offset. However, the main disadvantage of this detector is its inability continuously to reduce the width of the pulses which activate the current source 11 and current sink 12 in the charge pump. This limitation lies with the bandwidth of the switching logic. For the detector to be precisely centred in the middle of its linear range, i.e. where the AC leakage is at a minimum, one requires infinitely narrow pulses activating the current source/sink in the charge pump. In order to achieve such pulses one would have to have an infinite bandwidth. This is clearly impossible, and this inability to resolve very narrow pulses leads to a fall in the gain of the phase detector at the centre of its range. This region of low (or even zero) gain is commonly referred to as the "dead band" and is illustrated in Fig. 3 of the accompanying drawings. Operation in the "dead band" often leads to poor noise performance, but operation away from the "dead band" leads to AC leakage. Consequently, this known detector has considerable disadvantages.

It is an object of the present invention to provide a detector which overcomes or at least minimises the disadvantages of the known detectors referred to above.

In accordance with the invention there is provided a phase/frequency to voltage detector arranged to receive first and second input signals, logic circuit means connected to receive said first signal and to generate therefrom a third signal which is in phase with said first signal and a fourth signal which

gate means receiving said third and fourth signals and second gate means receiving said second and fourth signals, a current source and a current sink connected to the outputs of said first and second gate means, and charge-collecting means connected across the current source or current sink such that the net charge flowing into the charge-collecting means is the difference between the current source and the current sink over a given time period.

One presently preferred embodiment of detector in accordance with the invention will now be described by way of example and with reference to Figs. 4 to 6 of the accompanying drawings.

In the drawings:

Fig. 4 is a schematic representation of the detector;

Fig. 5 is a pulse diagram illustrating the operation of the detector of Fig. 4; and

Fig. 6 shows the transfer characteristics of the detector of Fig. 4.

As shown in Fig. 4, the detector of the present invention has two inputs i/p1 and i/p2. A logic circuit 13 of gates connected to input i/p1 generates two signals i and q. Signal i is in phase with i/p1 and signal q is in phase quadrature with i/p2. The signals are connected to gates A and B as shown, i.e. i and q to gate A and q and i/p2 to gate B. The output of gate A is connected to a current source I1. The output of gate B is connected to a current sink I2. A capacitor C is connected across the current sink, and the output O/P is taken from between the current source and the current sink.

The operation of the detector is shown logically in Fig. 5. If gate A is active high (1) then the current source I1 is turned on. If gate B is

then the current source I1 is turned on. If gate B is active high (1) then the current sink I2 is turned on. The current source I1 and current sink I2 are accurately matched in value.

When both inputs are in phase (Fig.5, case 3) both the current source I1 and the current sink I2 are on simultaneously, and thus the net charge into the capacitor C is zero. When input i/p1 is phase leading input i/p2 (Fig. 5, case 2) the current source I1 is turned on for longer than the current sink I2, by an amount which is proportional to the phase difference between input i/p1 and input i/p2. Consequently, there is a net positive flow of charge into the capacitor C. When input i/p1 is phase lagging input i/p2 (Fig. 5, case 1), the current sink I2 is held on for longer than the current source I1 by an amount which is proportional to the phase difference between input i/p1 and input i/p2. Consequently, there is a net flow of negative charge into the capacitor C.

The transfer characteristics of the detector circuit are shown in Fig. 6, where the DC output and the reference leakage are each shown plotted against phase difference.

Because the net charge flowing into the capacitor C is defined by the difference between a current source and a current sink over a given time period, infinitesimally small amounts of charge may be defined.

This technique in accordance with the present invention effectively overcomes the "dead band" problem of traditional digital tri-state detectors without compromising the AC reference leakage performance. It can thus be used with high speed inputs where low noise is required.

The detector of the present invention can be

implemented in a monolithic silicon integrated circuit. The detector has been found to work successfully with input frequencies of up to 2 MHz, and with no detectable "dead band".

CLAIMS:

1. A phase/frequency to voltage detector arranged to receive first and second input signals, logic circuit means connected to receive said first signal and to generate therefrom a third signal which is in phase with said first signal and a fourth signal which is in phase quadrature with said second signal, first gate means receiving said third and fourth signals and second gate means receiving said second and fourth signals, a current source and a current sink connected to the outputs of said first and second gate means, and charge-collecting means connected across the current source or current sink such that the net charge flowing into the charge-collecting means is the difference between the current source and the current sink over a given time period.

2. A detector as claimed in claim 1, in which the current source is connected to the output of said first gate means, the current sink is connected to the output of said second gate means, and the charge-collecting means is connected across the current sink, an output being taken from between the current source and the current sink.

3. A detector as claimed in claim 1 or 2, in which the charge-collecting means is a capacitor.

4. A phase/frequency to voltage detector substantially as hereinbefore described with reference to Figs. 4 to 6 of the accompanying drawings.

5. A phase locked loop synthesiser incorporating a phase/frequency to voltage detector as claimed in any preceding claim.